

PEAC: A Power-Efficient Adaptive Computing Technology for Enabling Swarm of Small Spacecraft and Deployable Mini-Payloads

Completed Technology Project (2012 - 2012)



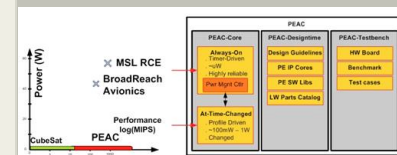
Project Introduction

This task is to develop and demonstrate a path-to-flight and power-adaptive avionics technology PEAC (Power Efficient Adaptive Computing). PEAC will enable emerging mission concepts that would otherwise be completely impossible such as formation flying and swarms or constellation of small spacecraft requiring low-power (tens of milli-watts to one-watt) typically powered only by primary batteries.

PEAC's novel technical approach is to leverage a low-power processor such as Aeroflex LEON-3 processor or ARM processor augmented with a co-processor, PEAC-Core, to be developed in this proposal that controls such critical system functions as power management, fault tolerance, and timing synchronization. It is based on observations of three major power-efficiency-limiting factors prevailing in conventional state-of-the-art space avionics: (1) Lack of adaptive, fine-grained, and multiple avionics power operational modes – almost all existing avionics designs support merely on/off power modes at the box-level. Once powered on, it is never powered off, wasting significant amount of energy even during off-duty cycle; (2) Lack of effective usage of inherent low-power features of modern space-grade microelectronics parts such as clock-gating and multiple-power-mode for microprocessors and variable-voltage-scaling for other parts; and (3) Lack of finer-granularity match between the mission operational mode (typically bursty) and the avionics operational mode (typically flat). PEAC's unique innovations are embodied in its three key components: (1) PEAC-Core: it is a central controller that handles power management, fault tolerance, and timing synchronization. It will provides on-demand and fine-grained power scheduling algorithm capable of trading performance and power consumption at run-time via systematic power management at both board and chip level. In particular, PEAC uses dual power domains: always-on domain – is always powered and provides minimal functions such as timer and CCSDS Critical Relay Command Handling, consumes minimal power of less than 100 μ W, and at-times-changed domain – it is managed at runtime with multiple power profiles adapted to various mission operational modes; (2) PEAC-designtime: it is a set of design guidelines of low-power board/firmware/software (such as clock gating, variable voltage scaling, etc.), power-aware RTL IP cores, power-aware.

Anticipated Benefits

None.



Project Image PEAC: A Power-Efficient Adaptive Computing Technology for Enabling Swarm of Small Spacecraft and Deployable Mini-Payloads

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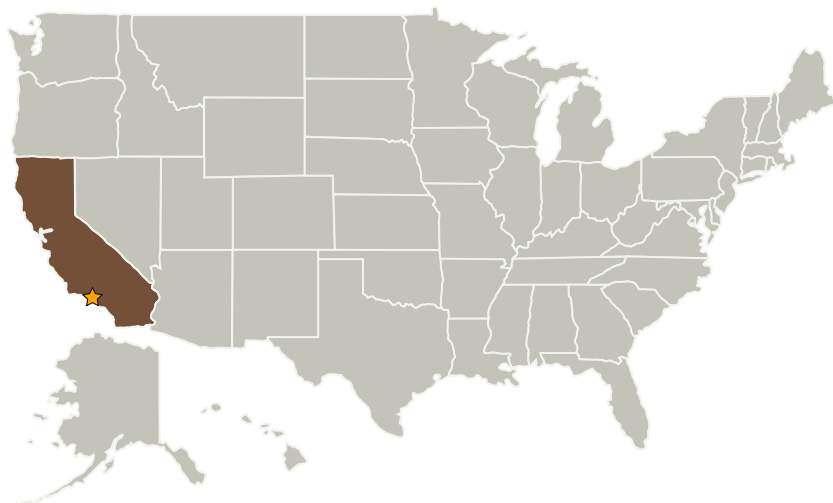
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Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
★ Jet Propulsion Laboratory (JPL)	Lead Organization	NASA Center	Pasadena, California

Primary U.S. Work Locations

California

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Center / Facility:

Jet Propulsion Laboratory (JPL)

Responsible Program:

Center Innovation Fund: JPL CIF

Project Management

Program Director:

Michael R Lapointe

Program Manager:

Fred Y Hadaegh

Project Manager:

Jonas Zmuidzinas

Principal Investigator:

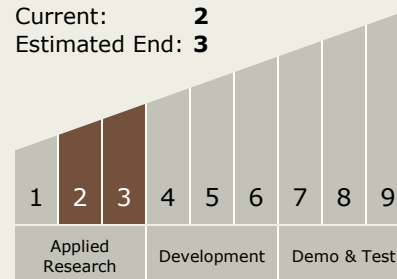
Yutao He

Technology Maturity (TRL)

Start: 2

Current: 2

Estimated End: 3

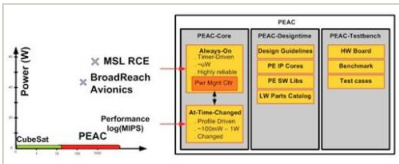


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Images



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Project Image PEAC: A Power-Efficient Adaptive Computing Technology for Enabling Swarm of Small Spacecraft and Deployable Mini-Payloads
(<https://techport.nasa.gov/image/1174>)

Technology Areas

Primary:

- TX03 Aerospace Power and Energy Storage
 - └ TX03.3 Power Management and Distribution
 - └ TX03.3.1 Management and Control